JP03116327 describes a high speed multiplier. Multiples of a first operand are pre-calculated and made available at a selector. The selection of the appropriate operand multiple is made according to the current pair of bits of the second operand. The selection requires the presence of both current bits of the second operand and only then can the addition operation be performed.

IN THE CLAIMS:

Please replace original 1-11 with new claims 12-18 as follows:

12. (new) A serial binary multiplier for multiplying two binary operands in two's complement form to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving bits of a second operand serially, a calculation unit comprising an adder and a subtractor for selectively adding or subtracting the element of the first operand to or from the partial product, means for selecting either the result output from the calculation unit or the currently stored partial product on the basis of the second operand and entering it into the partial product register, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

13. (new) A serial binary multiplier according to claim 1 , wherein the calculation unit is a single circuit capable of addition and subtraction operations, the operation being determined by the value of the previously received bit of the second operand.

14. (new) A serial binary multiplier according to claim 1, the add or subtract operation of the calculation unit is performed simultaneously with transmission of the current data bit of the second operand.

15. (new) A serial binary multiplier according to claim 1, wherein the mean for selecting is a decoder.

16. (new) A method of operating a serial binary multiplier for multiplying two binary operands in two's compliment form to provide a final product compromising the steps of storing a first operand, storing a partial product in a register, transmitting

bits of a second operand serially whilst simultaneously adding or subtracting the first operand to or from the partial product, selecting either the result from the addition or subtraction or the currently stored partial product on the basis of the value of the received bit of the second operand and entering it into the partial product register, shifting the partial product in the register to provide a new partial product, and outputting the contents of the register as the final product when all bits of the second operand have been received.

17. (new) A method according to claim 5, wherein the adding or subtracting operation is selected in response to the value of the previously received bit of the second operand.

18. (new) A method according to claim 5, wherein the adding or subtracting operation is performed simultaneously with transmission of the current data bit of the second operand.

Remarks:

Prior to the first Office Action, please enter the above amendments to the application and claims.

Respectfully submitted,

Dated: June 1, 2001

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